

# Compal Confidential

## Schematics Document

NVIDIA TEGRA 250 Platform  
T20 + LPDDR2

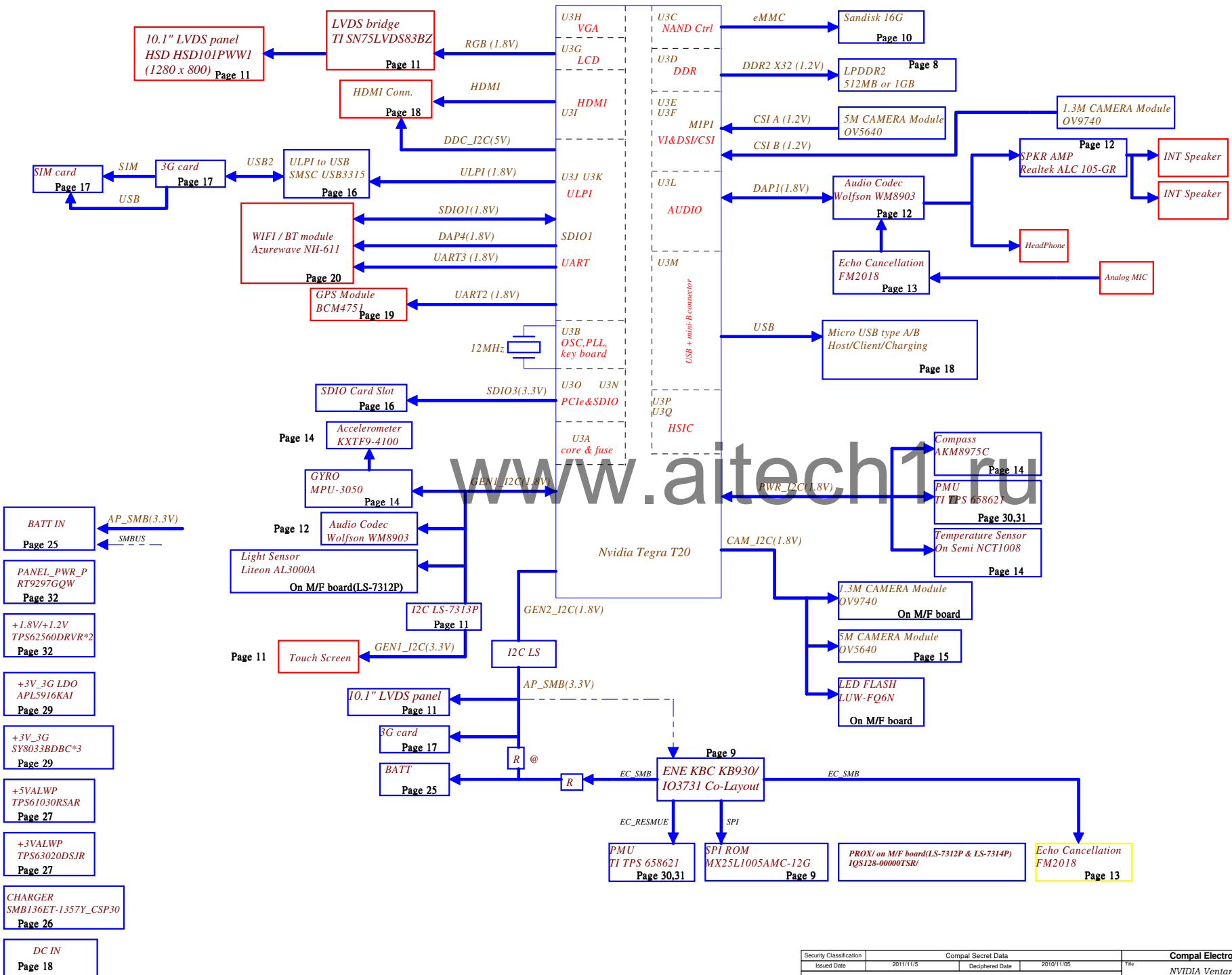
LA-7311P

2011-02-24

REV: 0.2

www.rosefix.com

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2011/11/5		2010/11/05		Cover Page	
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Voltage Rails

Power Plane	Description
VIN	Adapter power supply (19V)
B+	AC or battery power rail for power circuit.
+1.2VS_SM0	Core voltage for CPU
+1.0VS_SM1	CPU voltage for CPU
+1.1VS_LDO1	AVDD_PLL power rail
+1.2VS_LDO2	T20 RTC power rail
+1.8VS_LDO4	T20 system power rail
+3.3VS_LDO3	T20 USB power rail
+2.85VS_LDO5	Core voltage for EMMC
+2.85VS_LDO6	Core voltage for CAMERA
+3.3VS_LDO7	T20 HDMI power rail
+1.8VS_LDO8	T20 HDMI PLL power rail
+2.85VS_LDO9	T20 DDR RX power rail
+3VALW	3.3V always on power rail
+3VS	3.3V switched power rail for standby mode
+5VALW	5V always on power rail
+1.8VS	1.8V always on power rail
+1.8VS_S3	1.8V switched power rail for standby mode
+3.3VS_RTC	RTC power

PWR\_I2C address

Device	Address
PMU	0110 100x b
E-Compass	
Temperature sensor	1001 100x b

CAM\_I2C address

Device	Address
CAMERA 5M	0110 110x b
CAMERA 1.3M	1001 000x b

GEN1\_I2C

Device	Address
Audio Codec	0011 010x b
Light sensor	1000 100x b
Gyro	1101 000x b

TS\_I2C

Device	Address
Touch Panel	0100 110x b

GEN2\_I2C

Device	Address
--------	---------

AP\_SMB

Device	Address
LCD	
3G CARD	
BATT	
LED FLASH	

EC\_SMB

Device	Address
Proximity Sensor	1000 100x b
Echo Cancellation	1100 000x b
BATT	

IME\_I2C

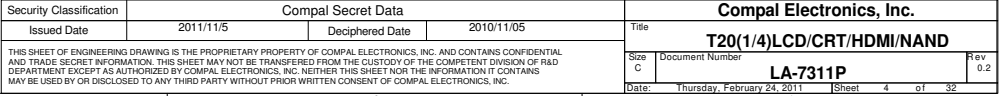
Device	Address
G-sensor	0001 111x b

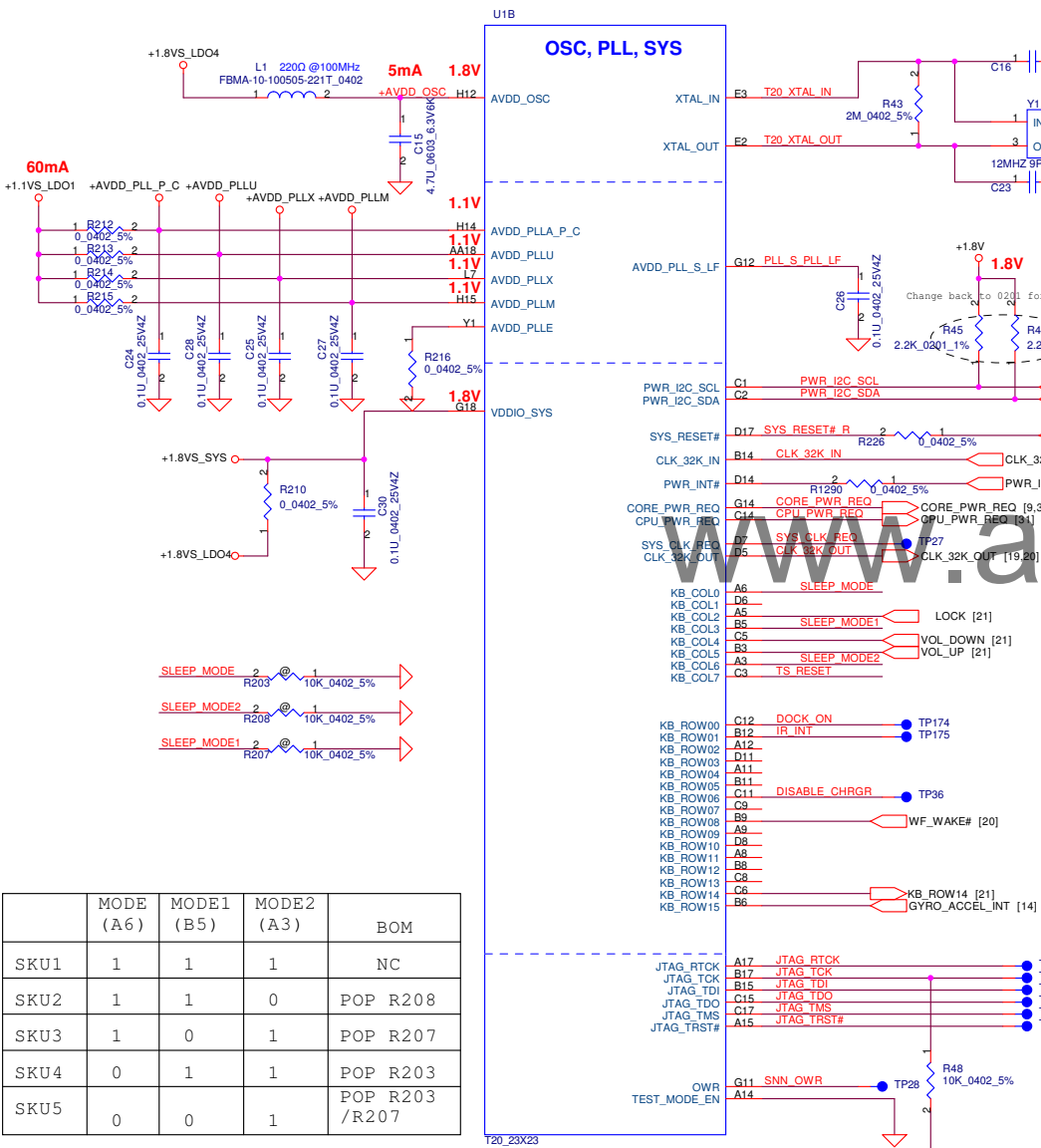
DDC\_I2C

Device	Address
--------	---------

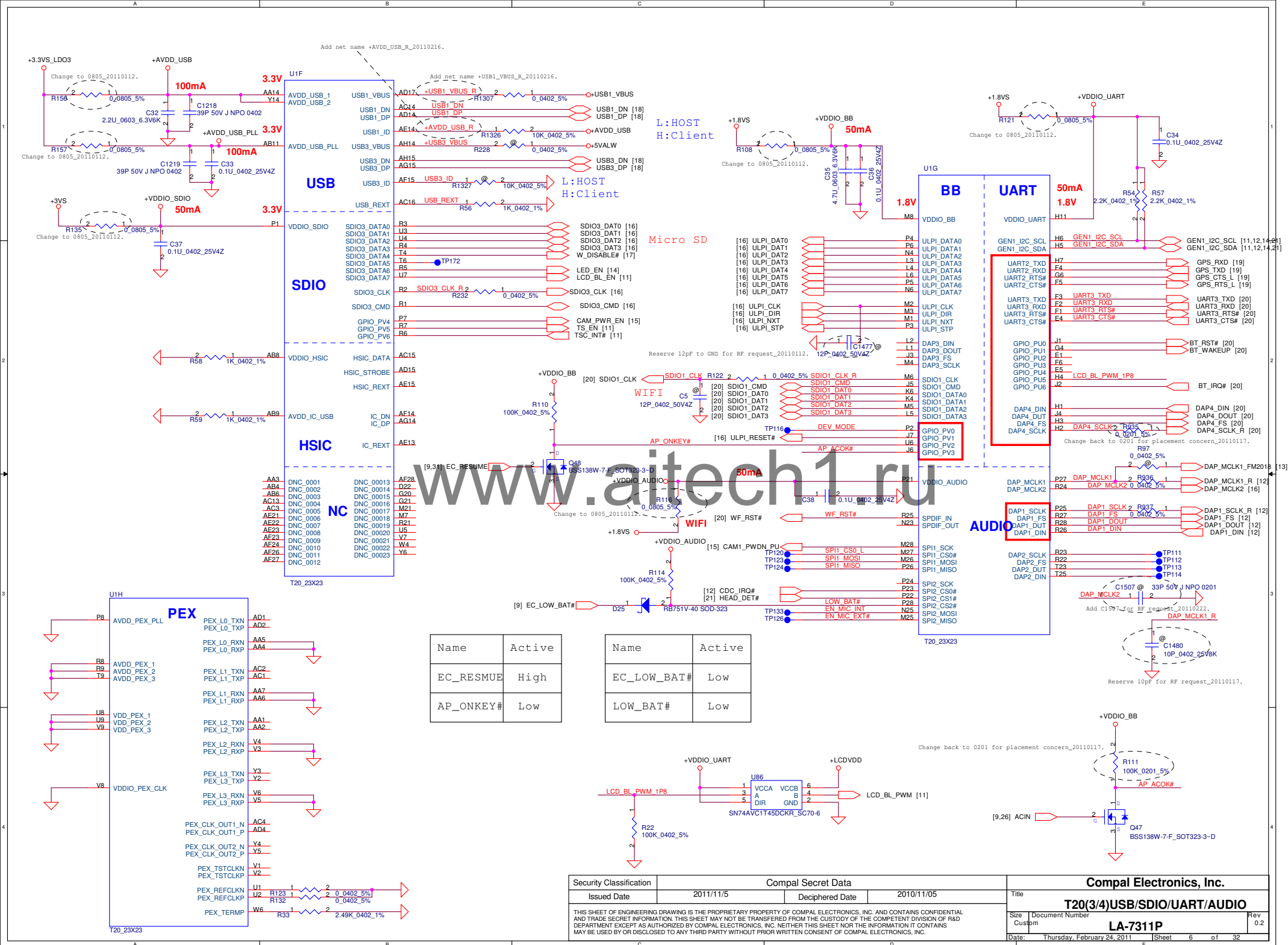
HDMI\_DDC\_I2C

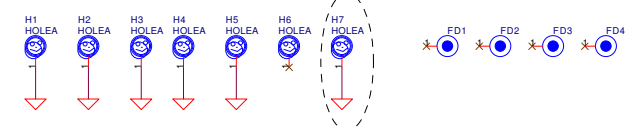
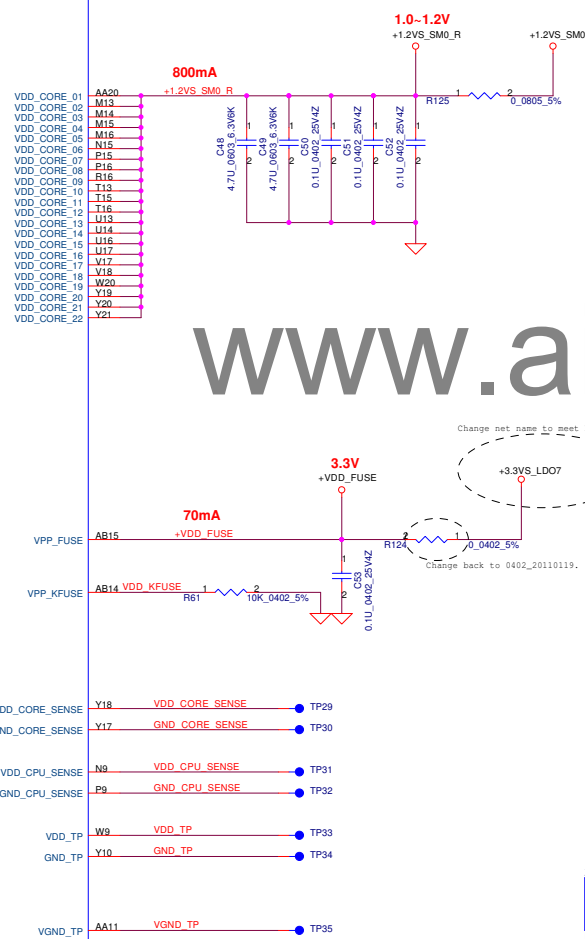
Device	Address
HDMI EDID	1010 000x b





	MODE (A6)	MODE1 (B5)	MODE2 (A3)	BOM
SKU1	1	1	1	NC
SKU2	1	1	0	POP R208
SKU3	1	0	1	POP R207
SKU4	0	1	1	POP R203
SKU5	0	0	1	POP R203 /R207



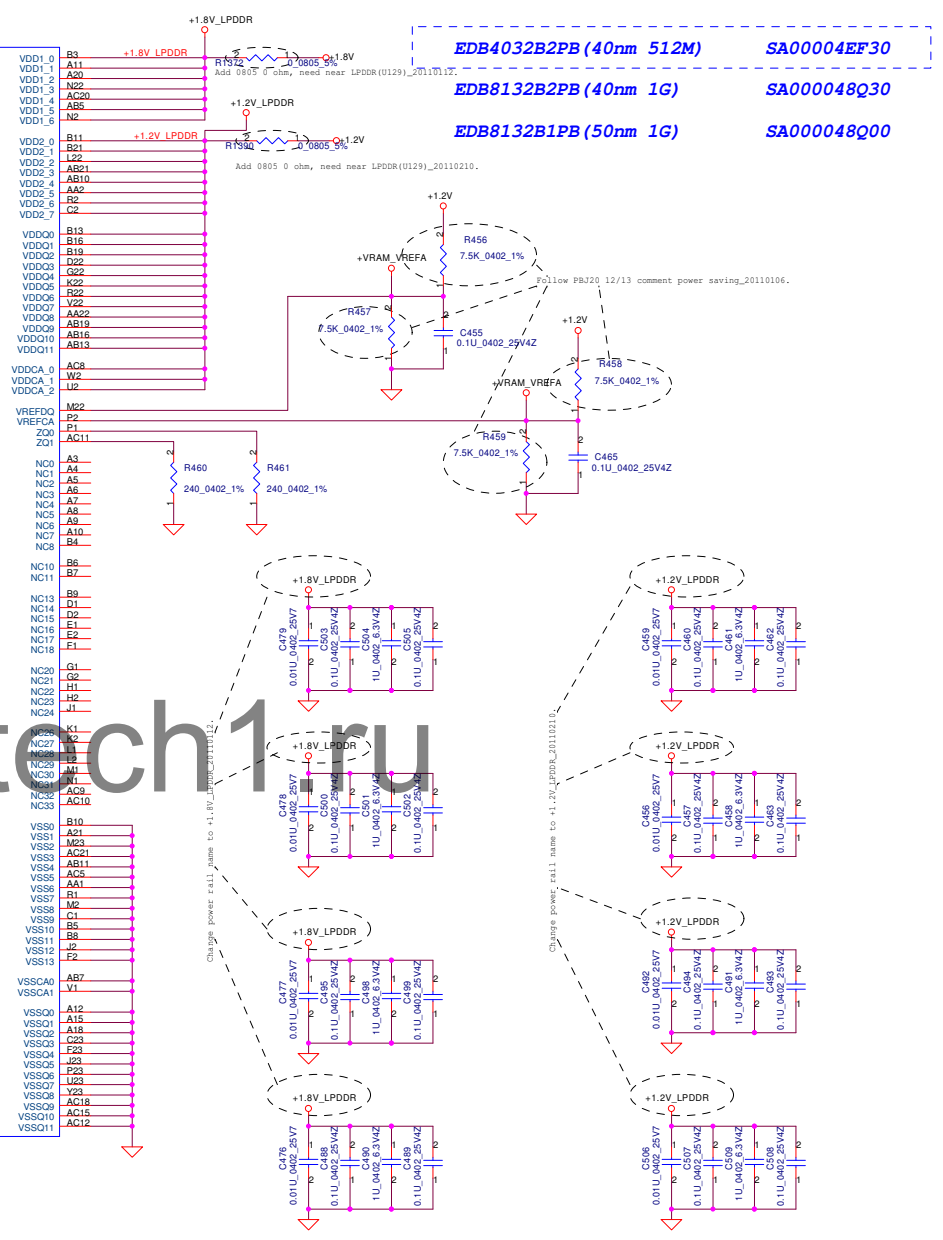


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					Size	Document Number	Rev	
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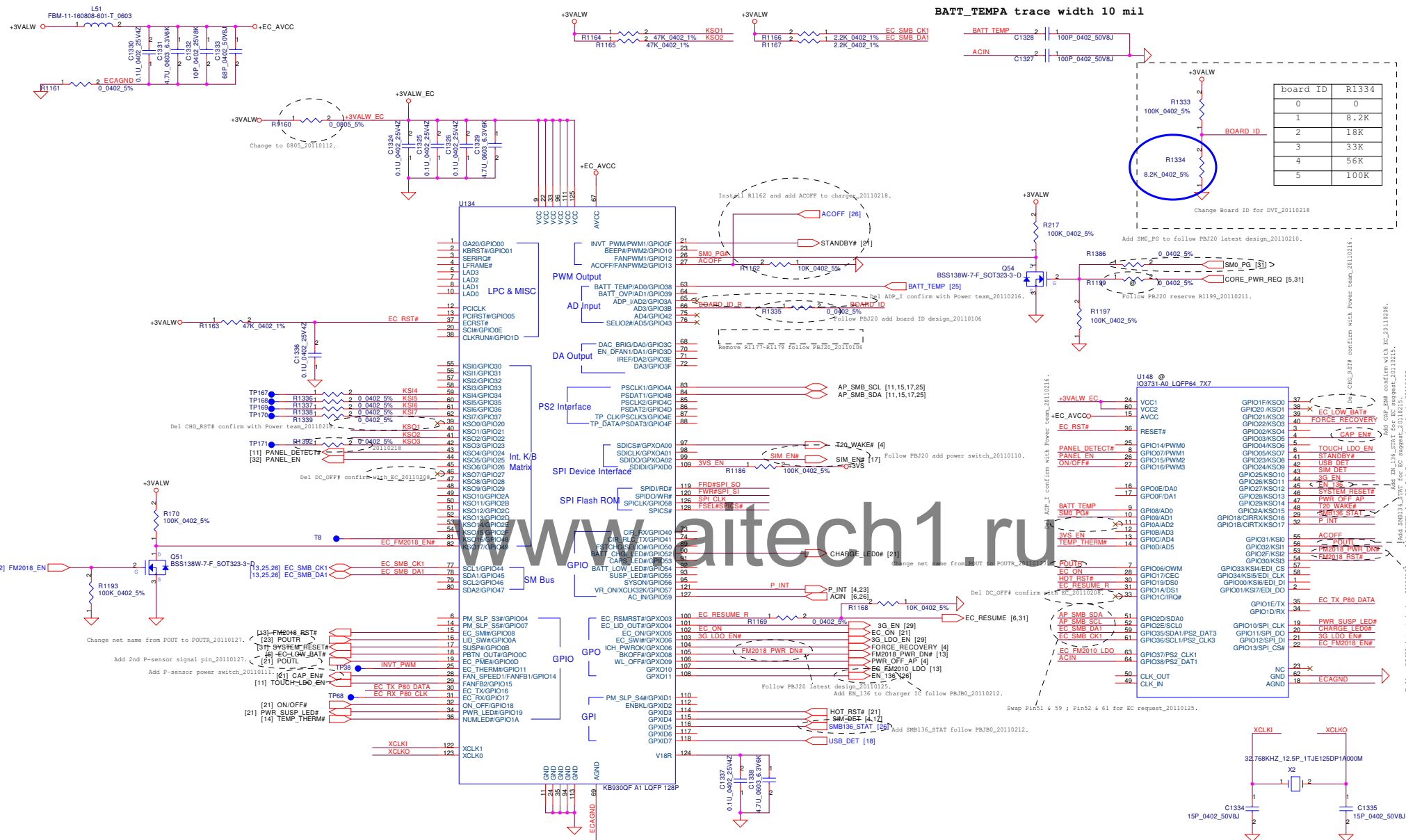
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[5] DDR_A_MA8	DDR_A_MA8	T2	CA8
[5] DDR_A_MA7	DDR_A_MA7	U1	CA7
[5] DDR_A_MA6	DDR_A_MA6	V2	CA6
[5] DDR_A_MA5	DDR_A_MA5	W1	CA5
[5] DDR_A_MA4	DDR_A_MA4	AB9	CA4
[5] DDR_A_MA3	DDR_A_MA3	AB8	CA3
[5] DDR_A_MA2	DDR_A_MA2	AC7	CA2
[5] DDR_A_MA1	DDR_A_MA1	AB6	CA1
[5] DDR_A_MA0	DDR_A_MA0	AC6	CA0
[5] M_CS#0	M_CS#0	AB3	CS0#
[5] M_CS#1	M_CS#1	AB4	CS1#
[5] M_CLK_DDR0	M_CLK_DDR0	Y2	CK
[5] M_CLK_DDR#0	M_CLK_DDR#0	V1	CK#
[5] M_CKE0	M_CKE0	AC3	CKE0
[5] M_CKE1	M_CKE1	AC4	CKE1
[5] DDR_A_DQS3	DDR_A_DQS3	B18	DQS3
[5] DDR_A_DQS#3	DDR_A_DQS#3	A19	DQS3#
[5] DDR_A_DQS2	DDR_A_DQS2	AB18	DQS2
[5] DDR_A_DQS#2	DDR_A_DQS#2	AC19	DQS2#
[5] DDR_A_DQS1	DDR_A_DQS1	J22	DQS1
[5] DDR_A_DQS#1	DDR_A_DQS#1	K23	DQS1#
[5] DDR_A_DQS0	DDR_A_DQS0	R23	DQS0
[5] DDR_A_DQS#0	DDR_A_DQS#0	P22	DQS0#
[5] DDR_A_DM3	DDR_A_DM3	B20	DM3
[5] DDR_A_DM2	DDR_A_DM2	AB20	DM2
[5] DDR_A_DM1	DDR_A_DM1	L23	DM1
[5] DDR_A_DM0	DDR_A_DM0	N23	DM0
[5] DDR_A_D31	DDR_A_D31	B12	DQ31
[5] DDR_A_D30	DDR_A_D30	A13	DQ30
[5] DDR_A_D29	DDR_A_D29	B14	DQ29
[5] DDR_A_D28	DDR_A_D28	B15	DQ28
[5] DDR_A_D27	DDR_A_D27	A16	DQ27
[5] DDR_A_D26	DDR_A_D26	A17	DQ26
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[5] DDR_A_D24	DDR_A_D24	B17	DQ24
[5] DDR_A_D23	DDR_A_D23	AC17	DQ23
[5] DDR_A_D22	DDR_A_D22	AB17	DQ22
[5] DDR_A_D21	DDR_A_D21	AC16	DQ21
[5] DDR_A_D20	DDR_A_D20	AB15	DQ20
[5] DDR_A_D19	DDR_A_D19	AC14	DQ19
[5] DDR_A_D18	DDR_A_D18	AB14	DQ18
[5] DDR_A_D17	DDR_A_D17	AC13	DQ17
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[5] DDR_A_D15	DDR_A_D15	C22	DQ15
[5] DDR_A_D14	DDR_A_D14	D23	DQ14
[5] DDR_A_D13	DDR_A_D13	E22	DQ13
[5] DDR_A_D12	DDR_A_D12	F22	DQ12
[5] DDR_A_D11	DDR_A_D11	G23	DQ11
[5] DDR_A_D10	DDR_A_D10	H23	DQ10
[5] DDR_A_D9	DDR_A_D9	H22	DQ9
[5] DDR_A_D8	DDR_A_D8	I22	DQ8
[5] DDR_A_D7	DDR_A_D7	J23	DQ7
[5] DDR_A_D6	DDR_A_D6	I22	DQ6
[5] DDR_A_D5	DDR_A_D5	J22	DQ5
[5] DDR_A_D4	DDR_A_D4	V23	DQ4
[5] DDR_A_D3	DDR_A_D3	W23	DQ3
[5] DDR_A_D2	DDR_A_D2	W22	DQ2
[5] DDR_A_D1	DDR_A_D1	Y22	DQ1
[5] DDR_A_D0	DDR_A_D0	AB23	DQ0

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MT46H64M32L2JG-51T-A\_FPGA168





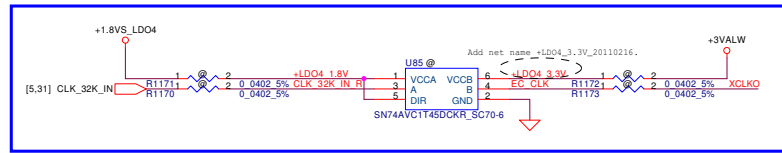
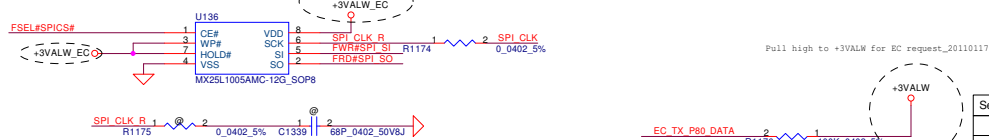


board ID	R1334
0	0
1	8.2K
2	18K
3	33K
4	56K
5	100K

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## BIOS

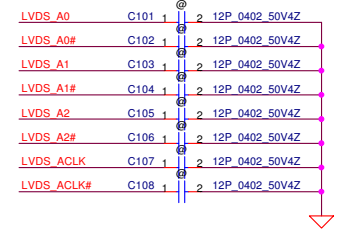
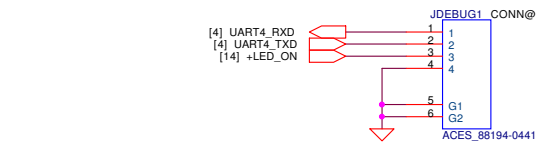
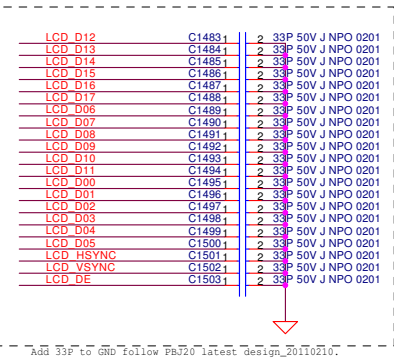
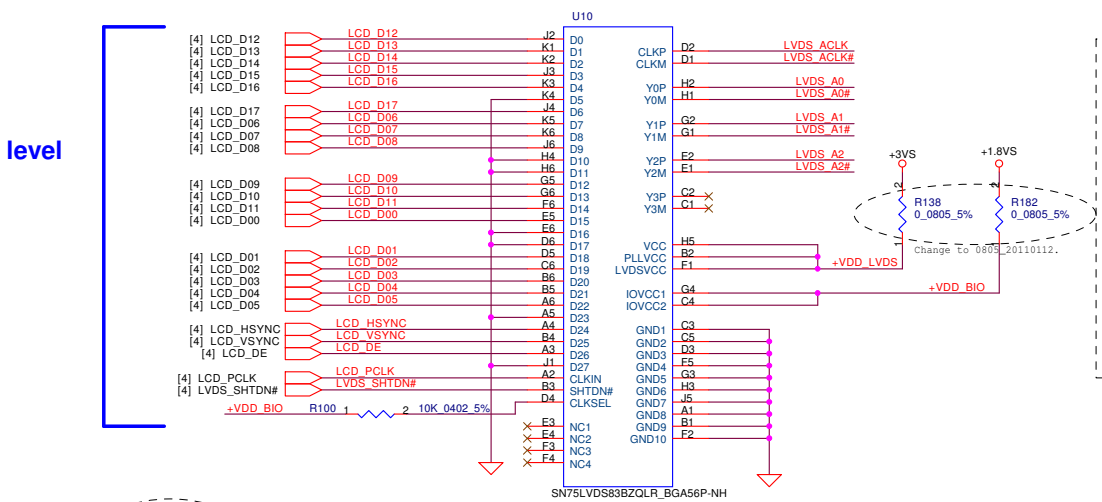
Change net name from +3VALW to +3VALW\_EC\_20110212.



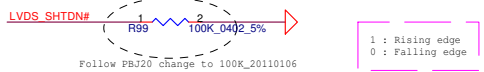
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1.8V level



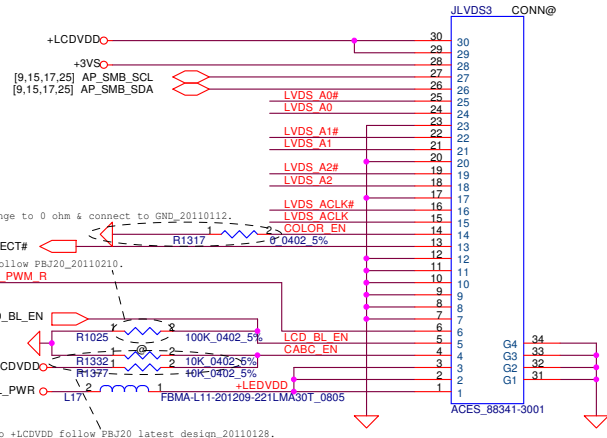
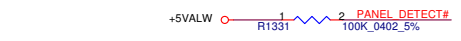
Note: PANEL\_DETECT# connect to PANEL GND pin



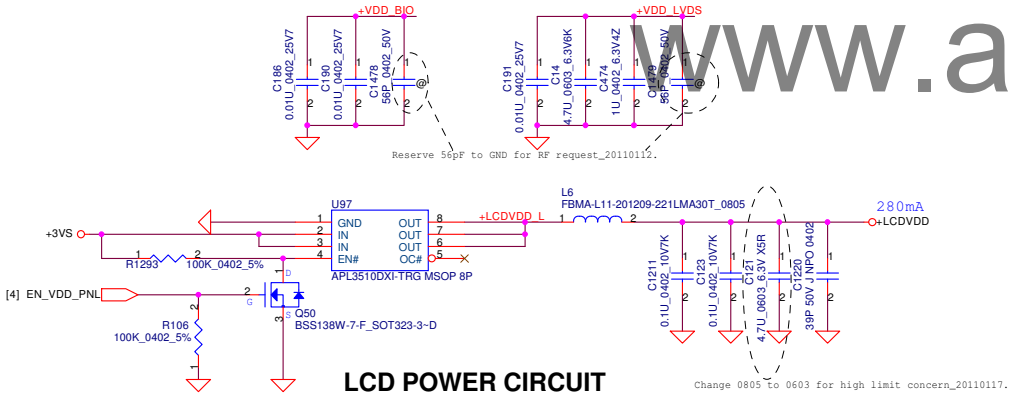
LVDS Bridge

1 : Rising edge  
0 : Falling edge

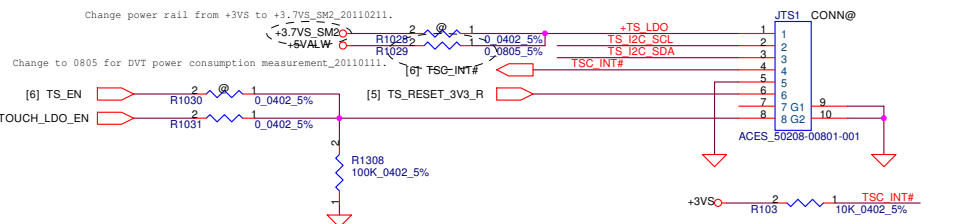
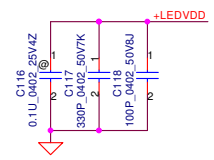
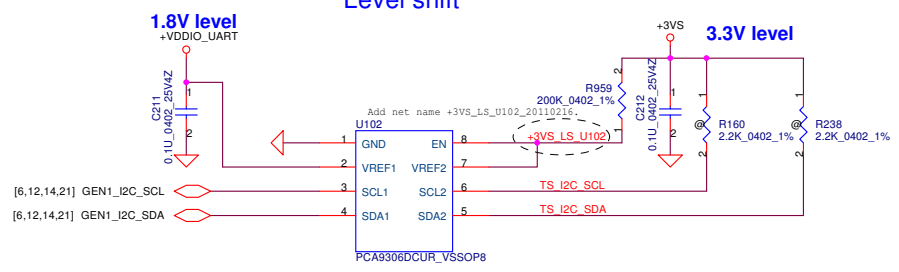
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LCD POWER CIRCUIT

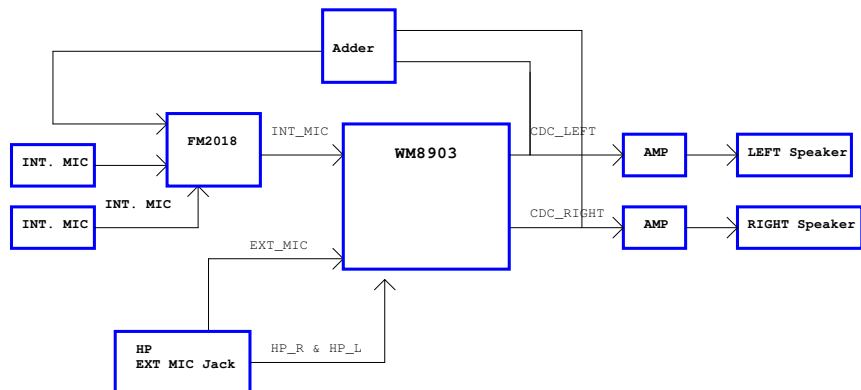
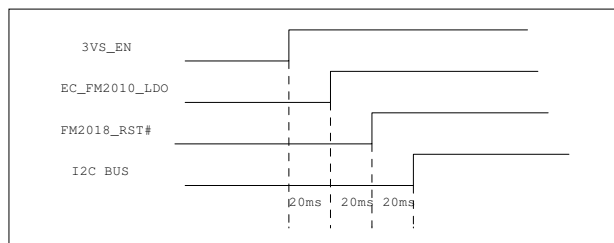
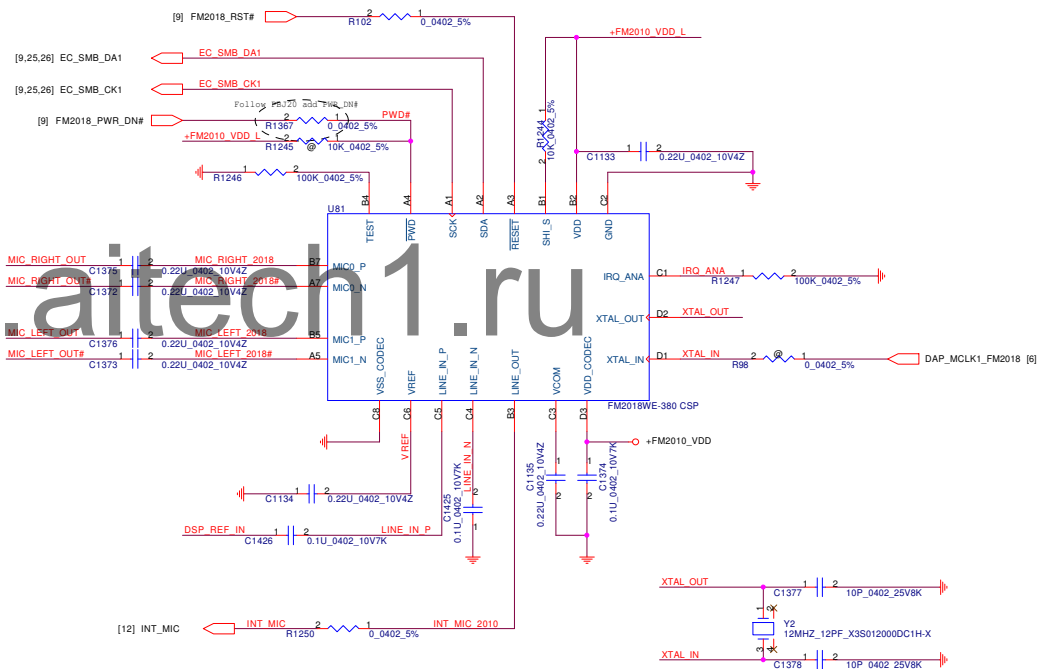
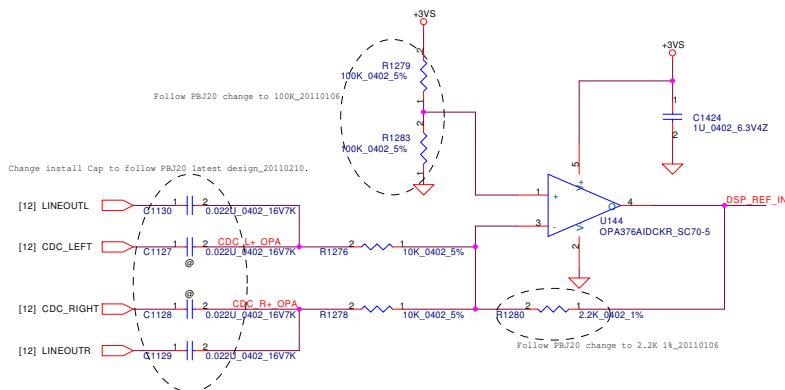
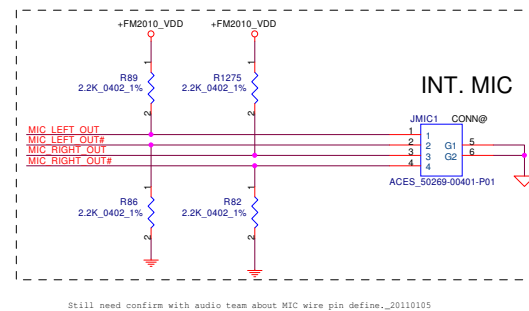


Level shift

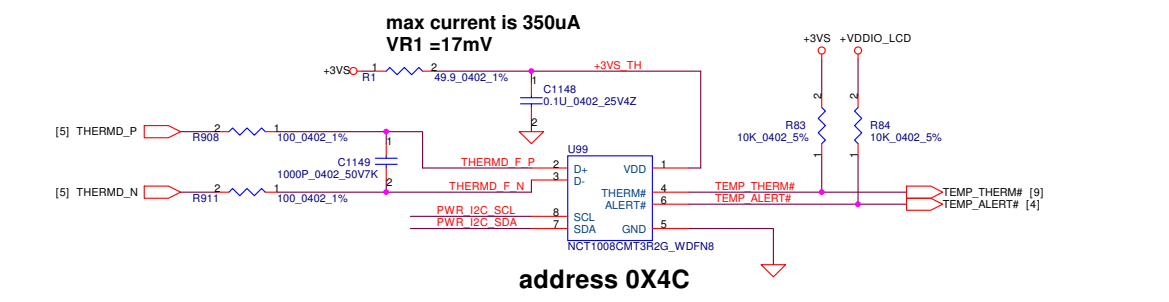
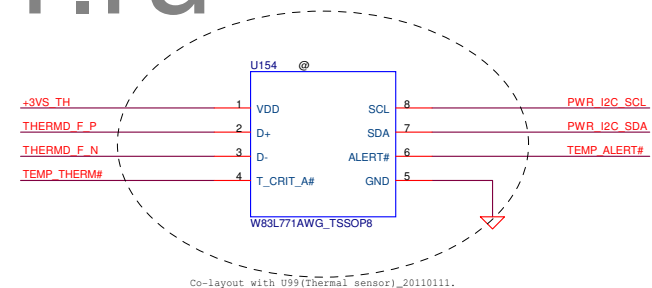
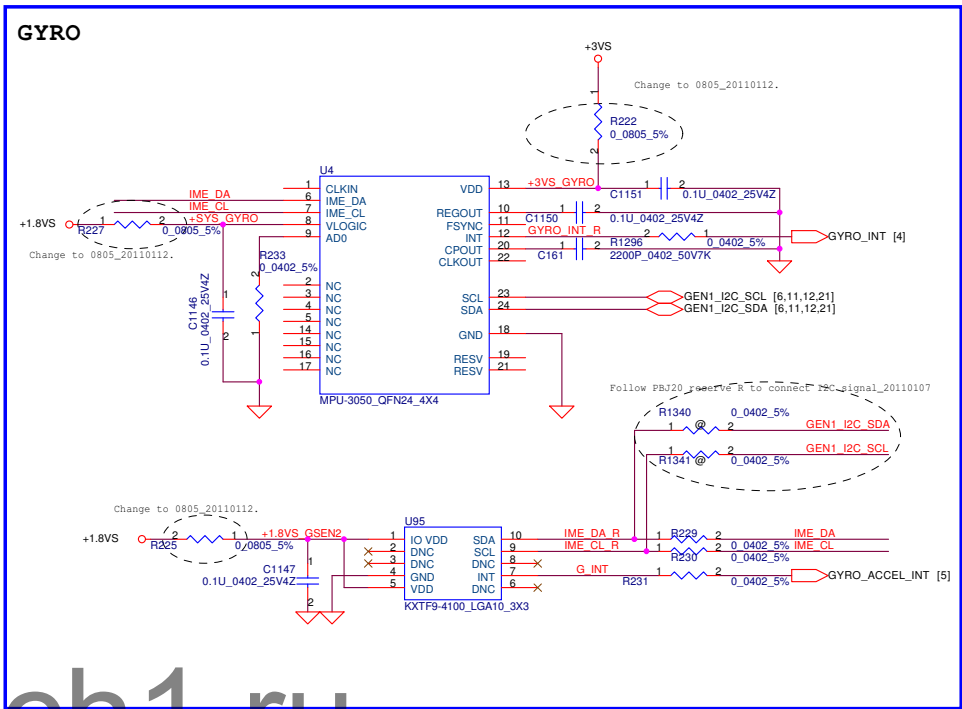
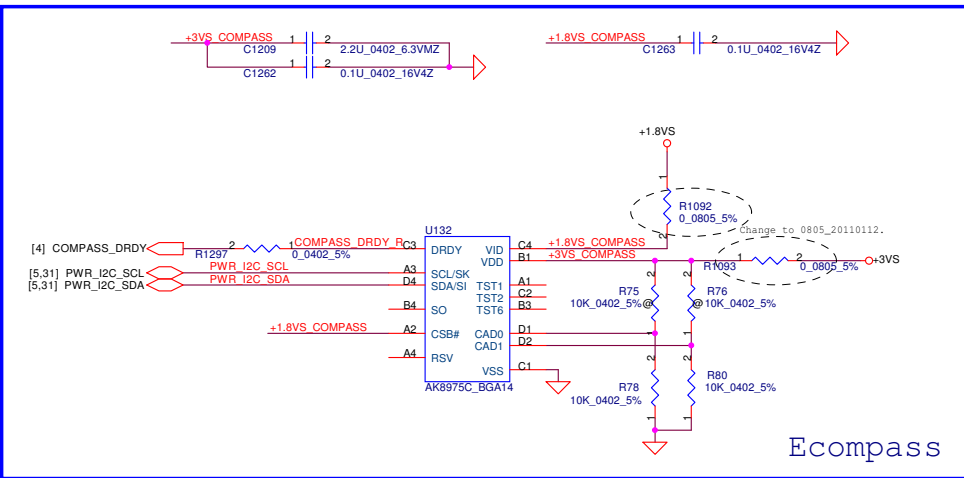
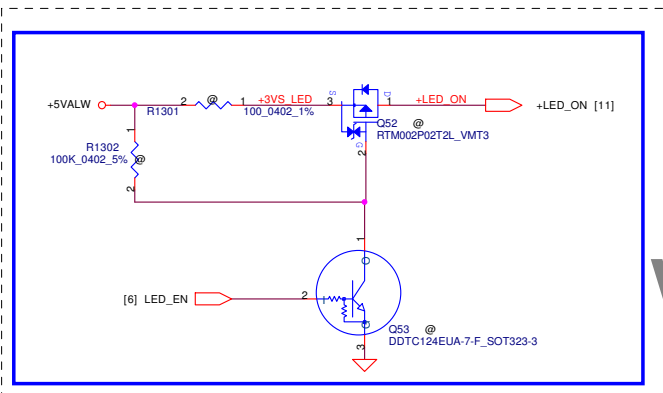


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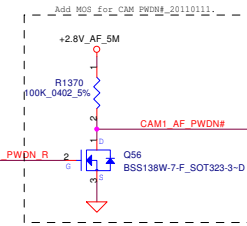
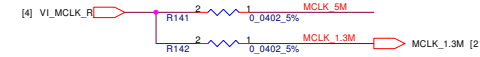
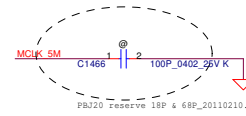
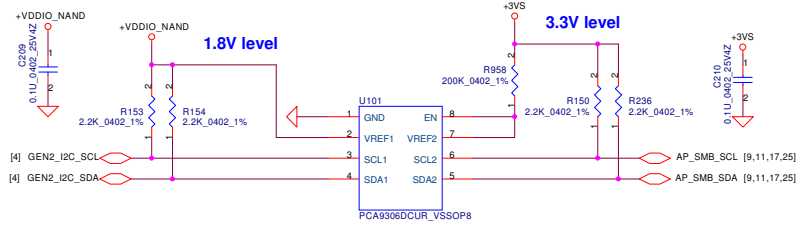


All component change to "@\_20110111.



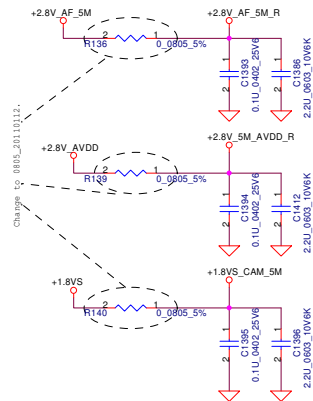
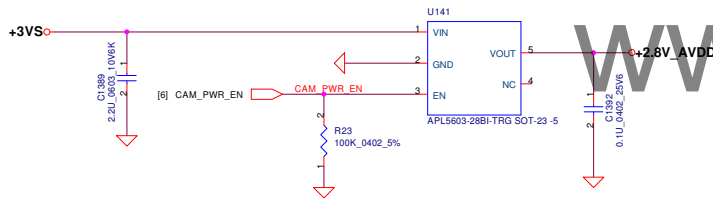
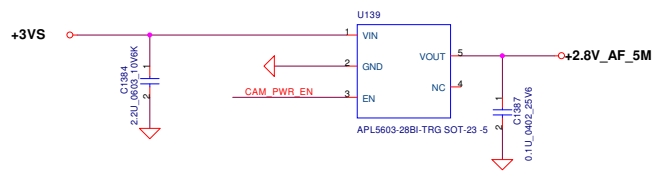
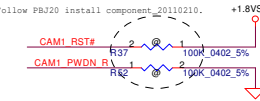
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## Level shift

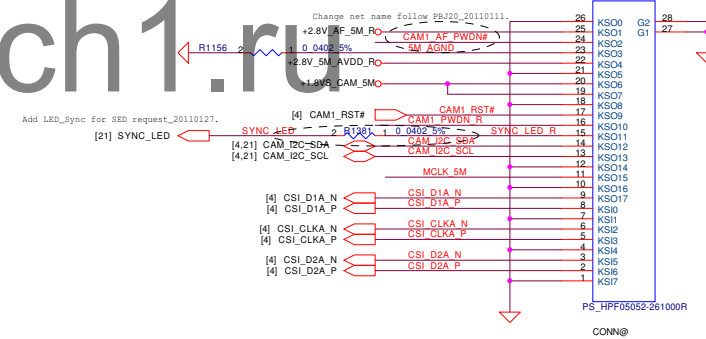


Name	Active
CAM1_RST#	Low
CAM1_PWDN_R	High

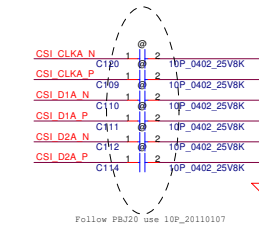
Follow PBJ20 install component\_20110210.



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5M connector

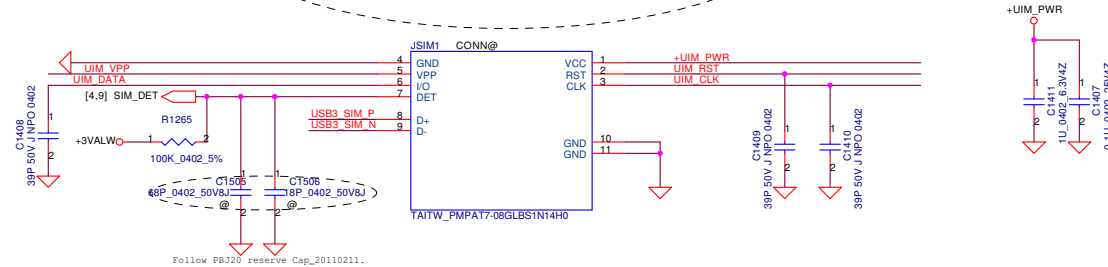


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Size	C	Document Number	LA-7311P
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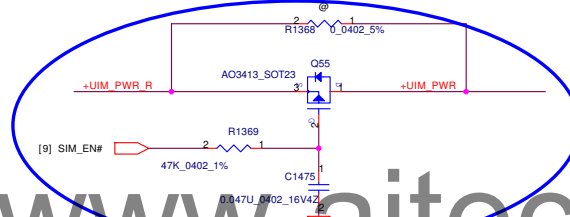


Remove D3 for EMI request\_20110121.



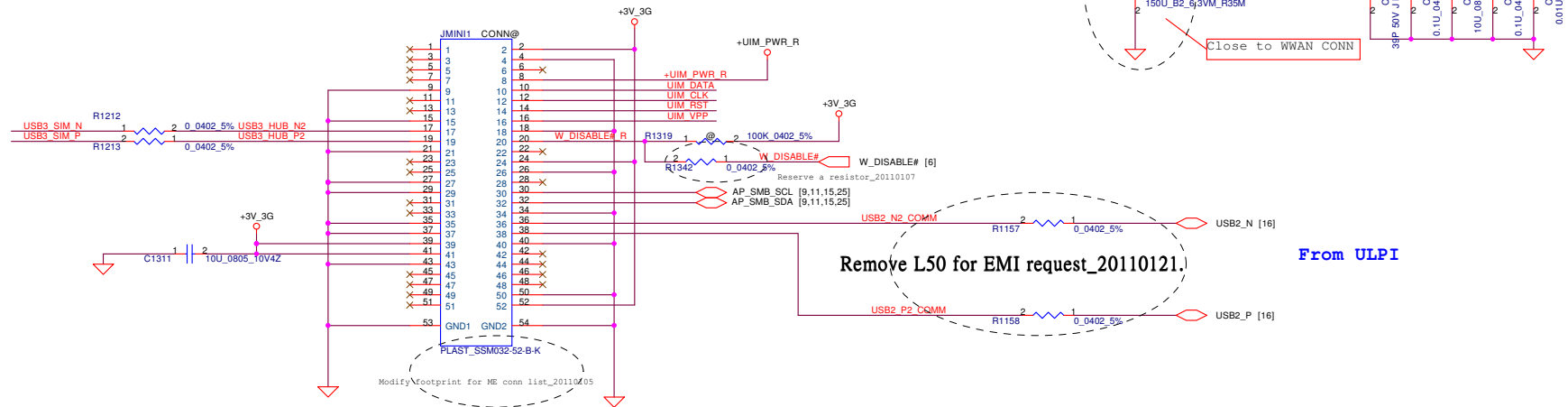
### SIM CARD

Follow PBJ20 design add SIM on/off circuit\_20110110.



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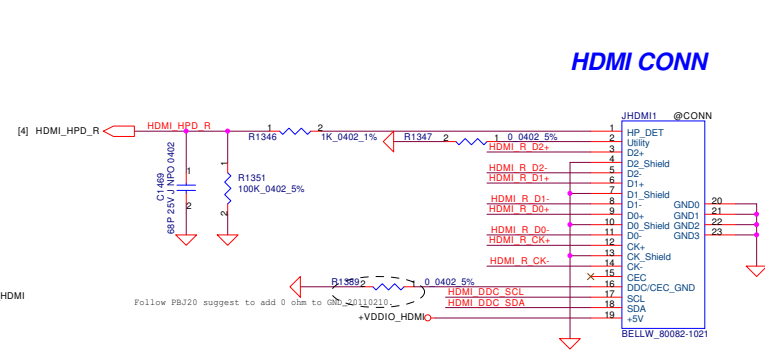
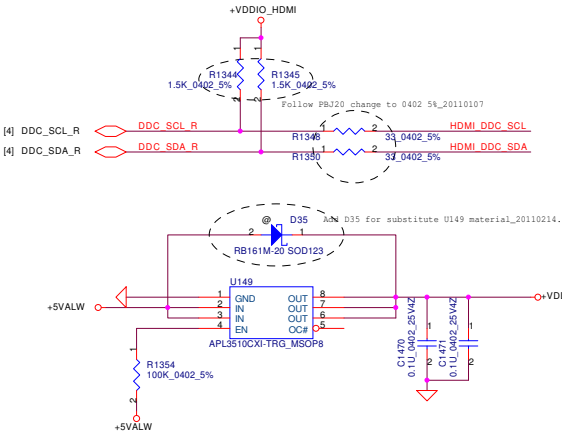
### Mini-Express Card for WWAN



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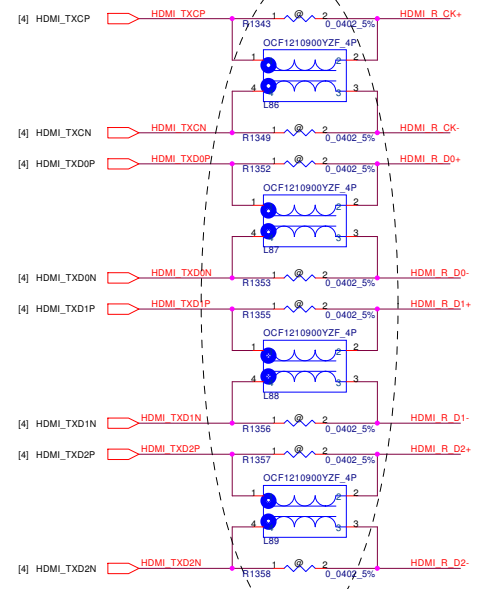
From ULPI

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					Date:	Thursday, February 24, 2011	Sheet

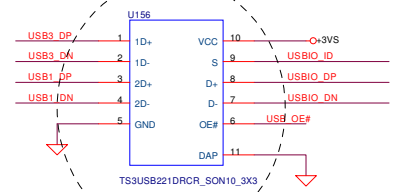
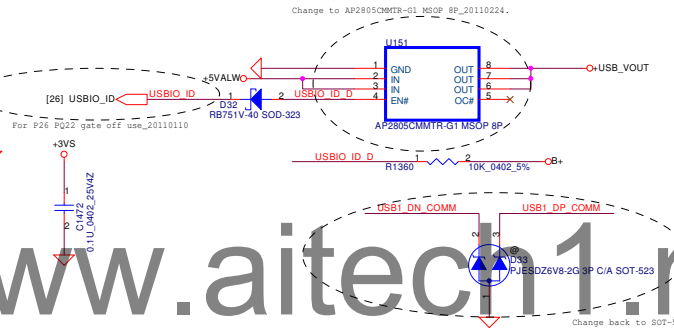
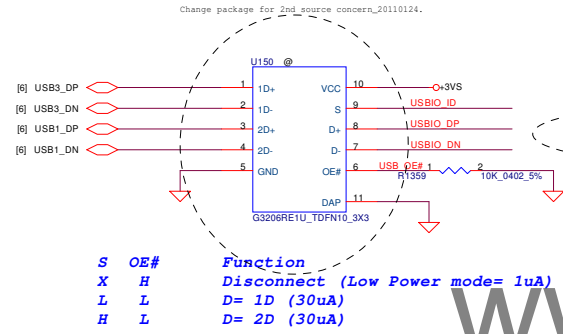


HDMI Type D Connector

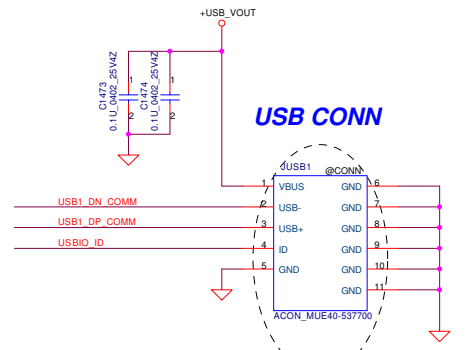
Update L86-L89 to 0504 package\_20110124.



Host T20 Port3  
Client T20 Port1

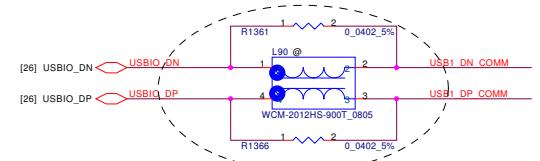
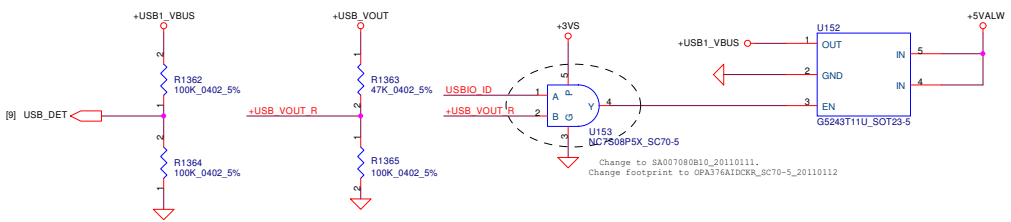


Co-layout USB MIX Switch\_20110218.



USB CONN

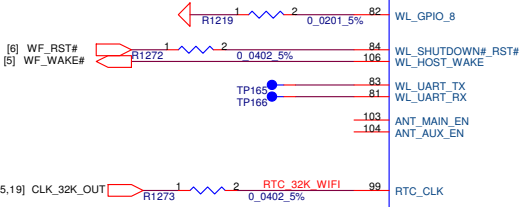
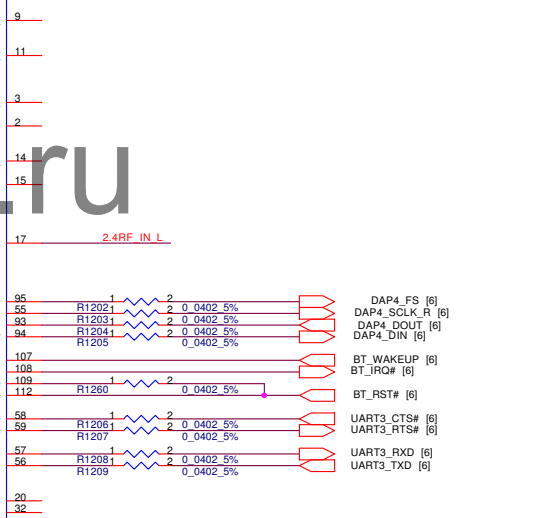
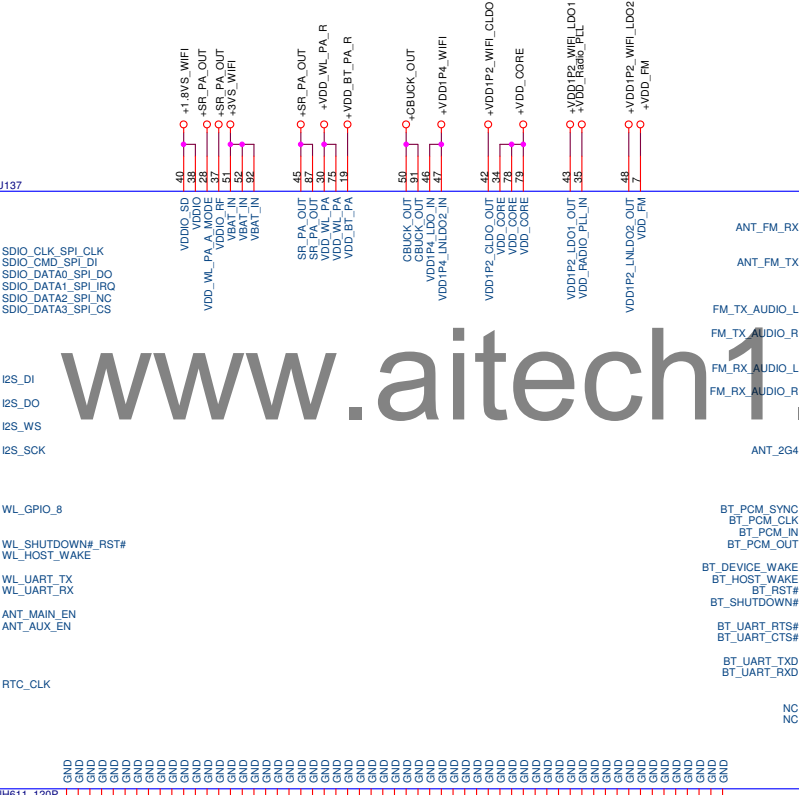
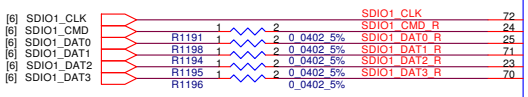
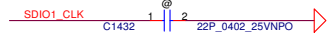
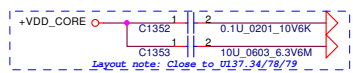
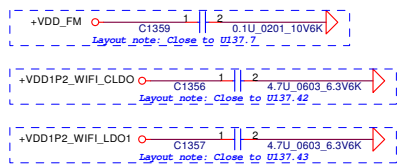
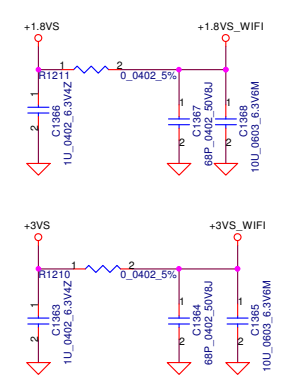
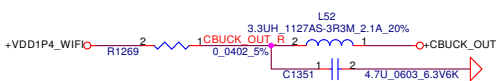
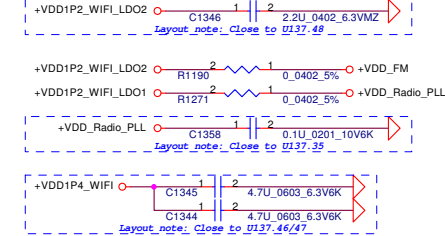
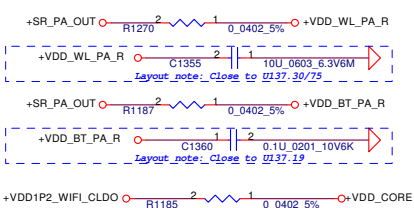
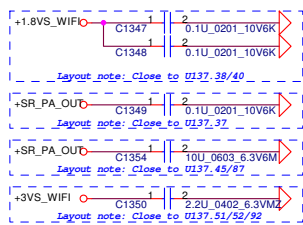
Change conn footprint\_20110221.



Install R1361 & R1366 ; Reserve L90 for EMI request\_20110121.

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				Date:	Thursday, February 24, 2011	Sheet 18 of 32



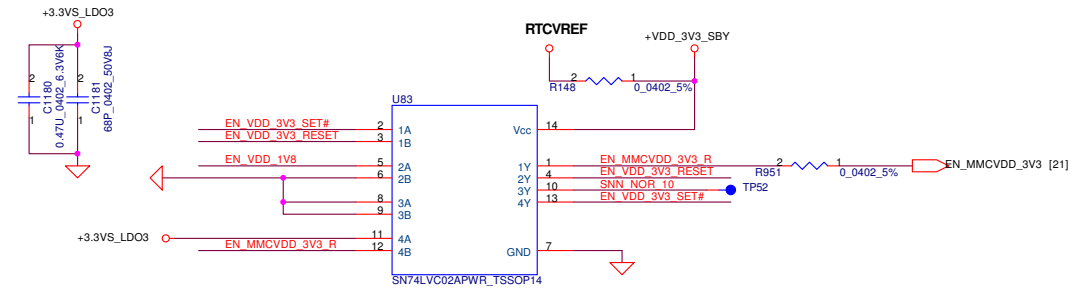


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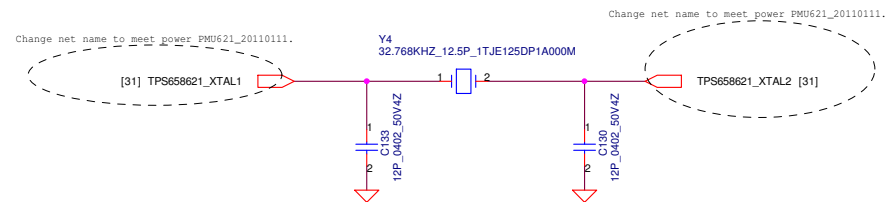
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The schematic diagram illustrates the pull-up circuit for the SN74AVC1T45DCKR\_SC70-6 chip. The circuit includes a pull-up resistor R131 connected to a +2.2VS supply. The signal line, labeled PG\_VDDIO\_SYS, is connected to the VCCA pin of the SN74AVC1T45DCKR\_SC70-6 chip. The chip's VCCB pin is connected to a +VDD\_3V3\_SBY supply, and its DIR pin is connected to the EN\_VDD\_1V8 signal. The chip's A pin is connected to the signal line, and its B pin is connected to GND. The signal line is also connected to the EN\_VDD\_1V8 signal.

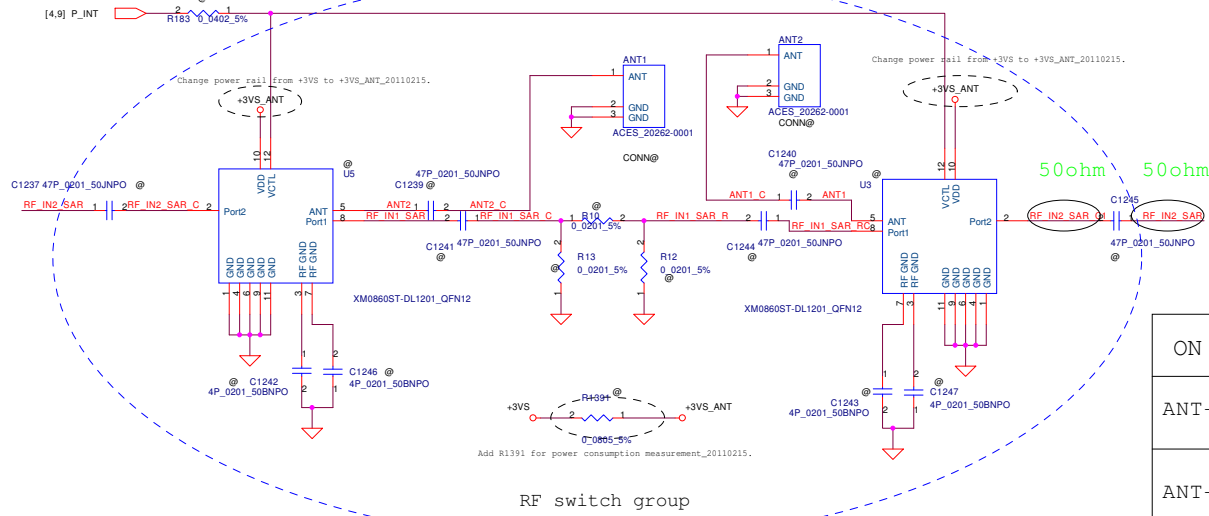


connect to PMU



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High active 20110218



ON PORT	VCTL
ANT-Port1	H
ANT-Port2	L

11/02 RF switch circuit Reserve RF switch circuit component\_20110221.

P4 already has the material.(R1316 & D30)

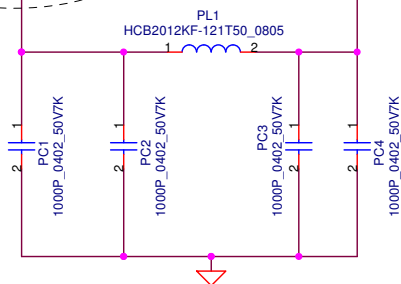
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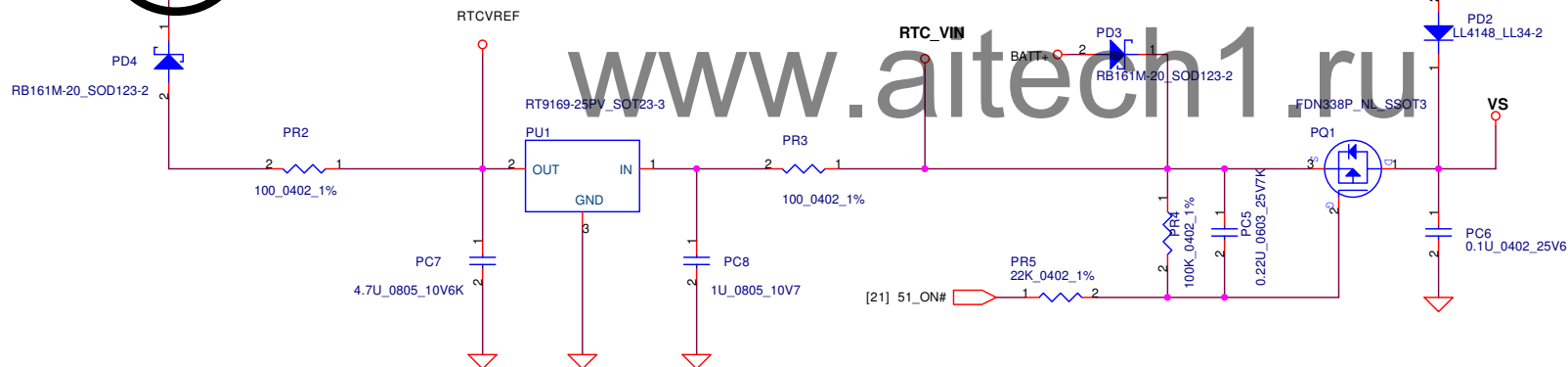
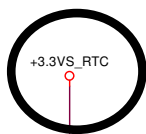
Change net name to meet USB(P18) net name\_20110110.

+USB\_VOUT

VIN



實口甯?.5V

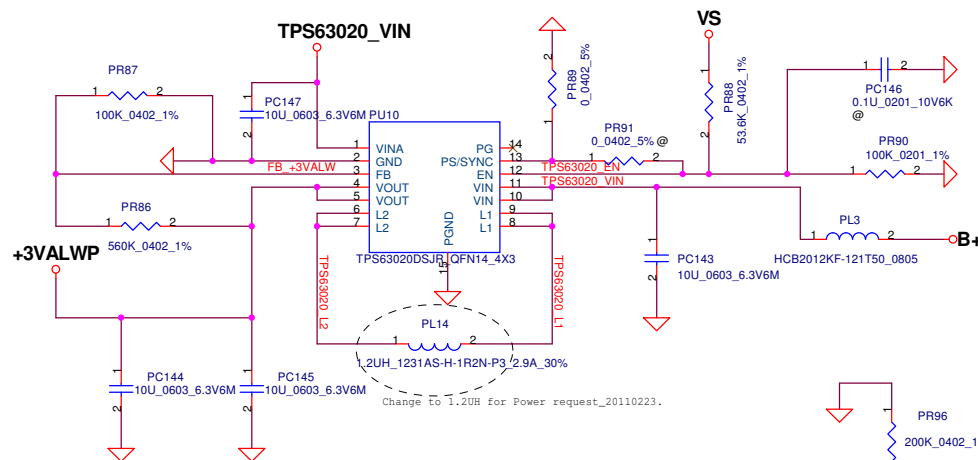


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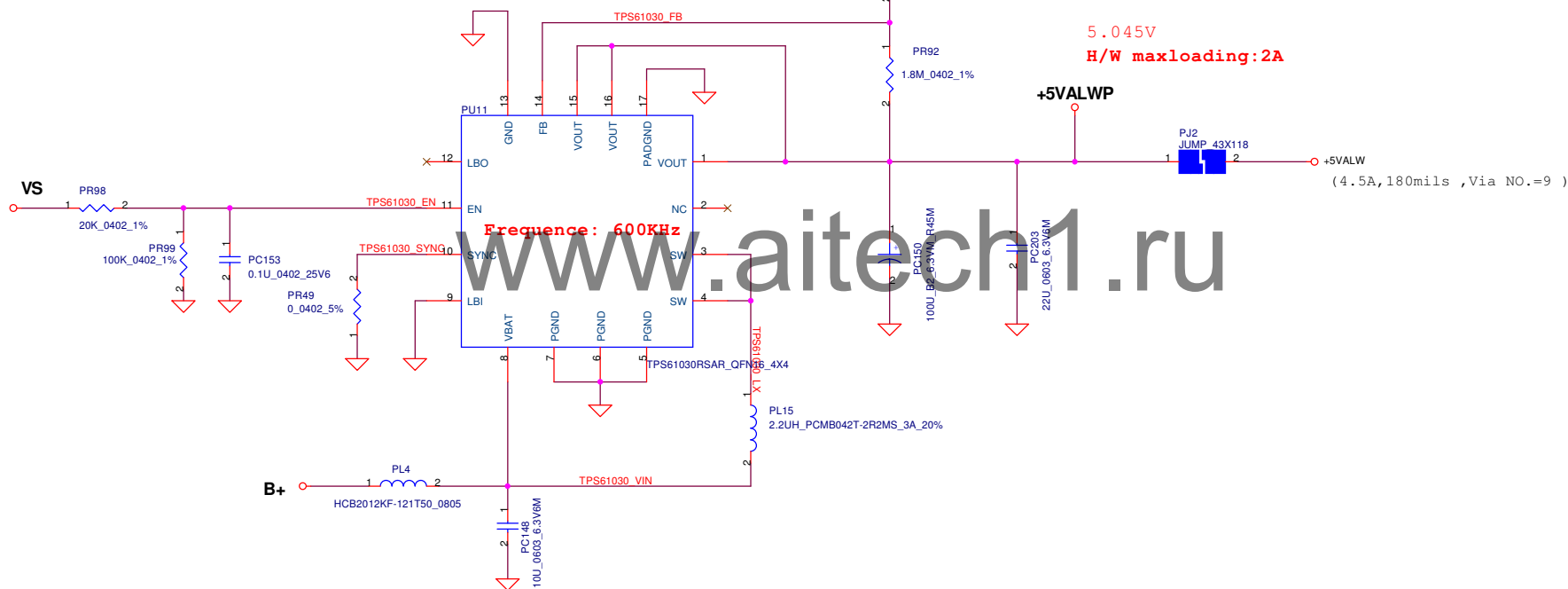
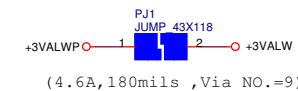


Imax=2A

$$V_o = 3.3 \text{ VS} \quad V_{FB} = 0.5V$$

$$V_o = V_{FB}(1 + R_{12}/R_{14})$$

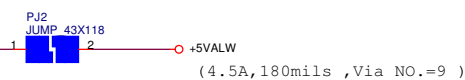
$$3.3 = 0.5(1 + 560/100)$$



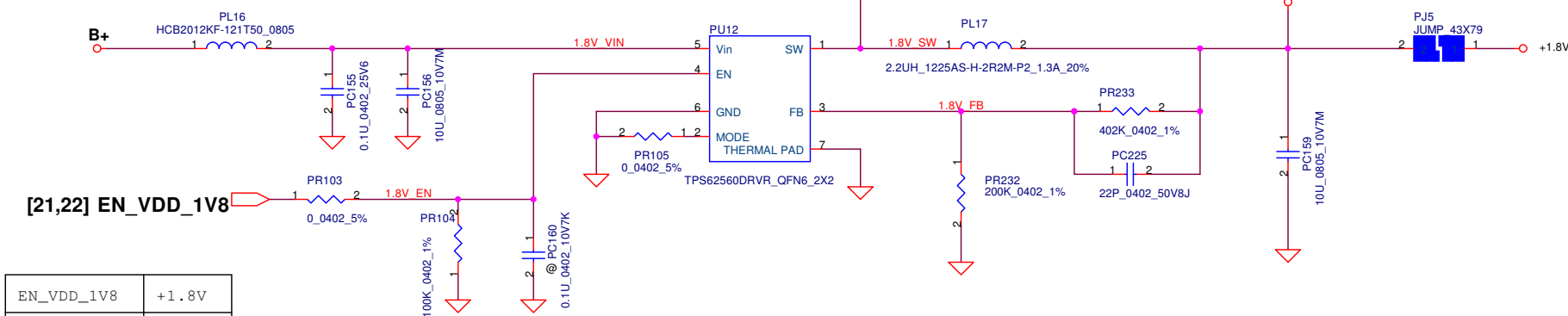
Frequency: 600KHz

5.045V

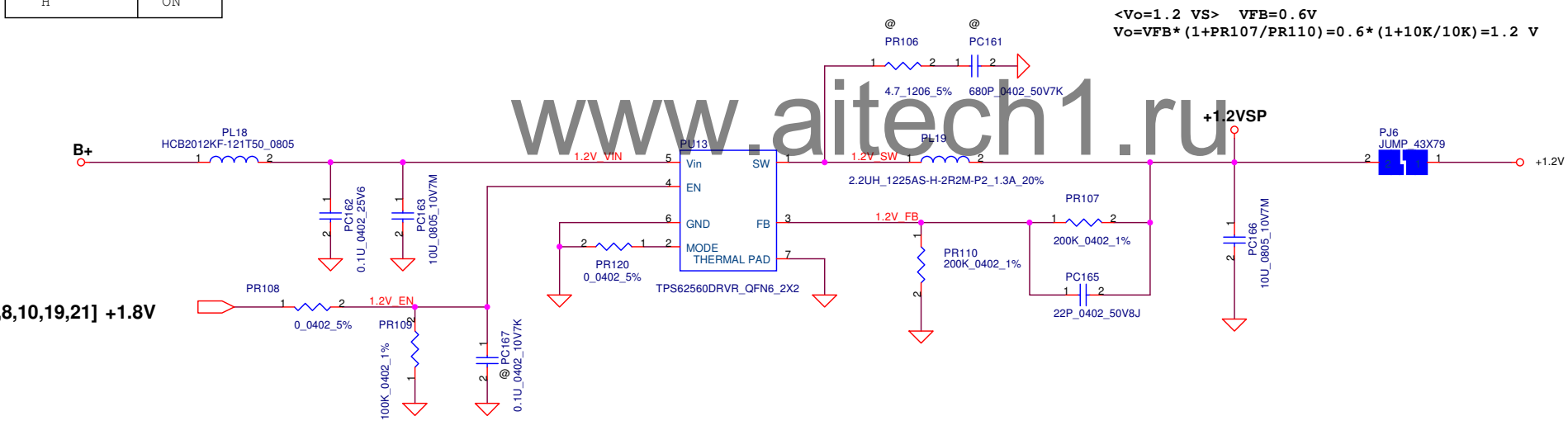
H/W maxloading:2A



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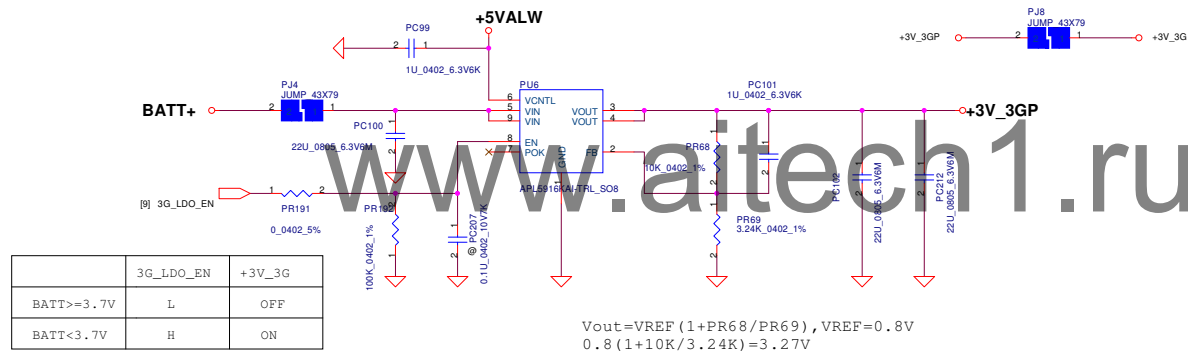
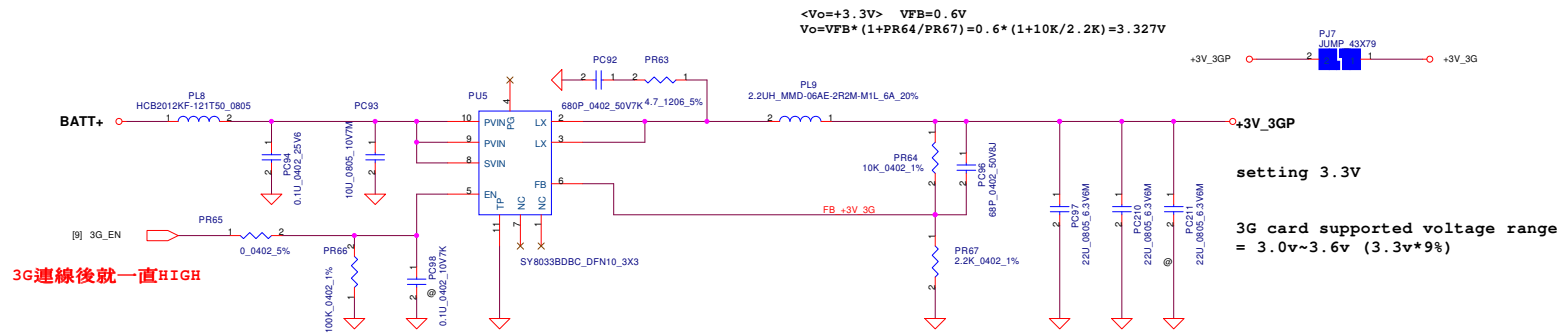


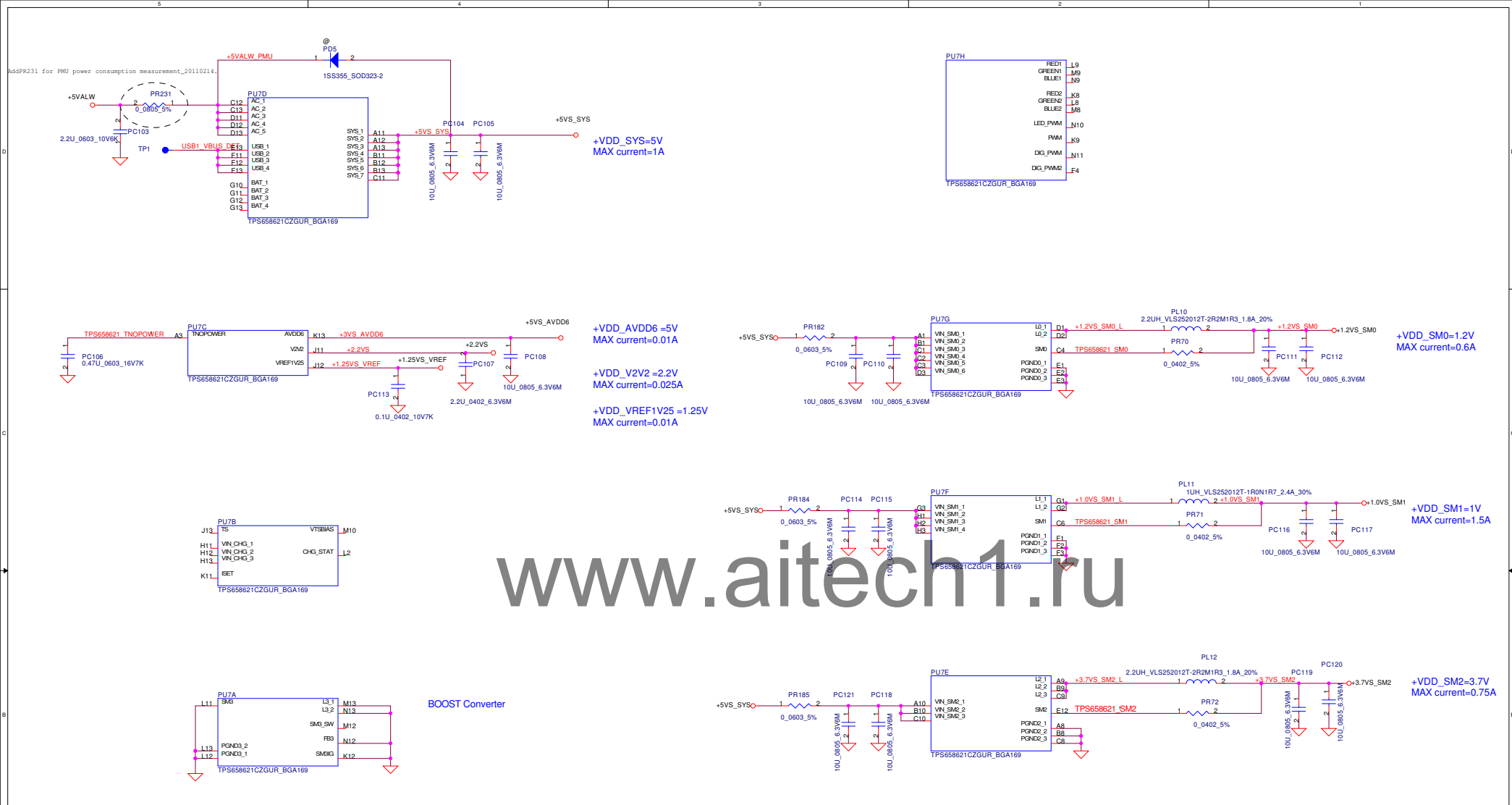
EN_VDD_1V8	+1.8V
L	OFF
H	ON



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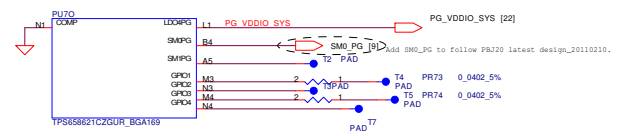
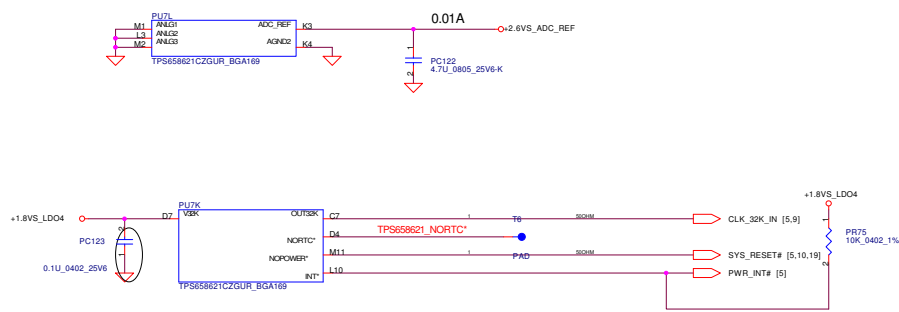




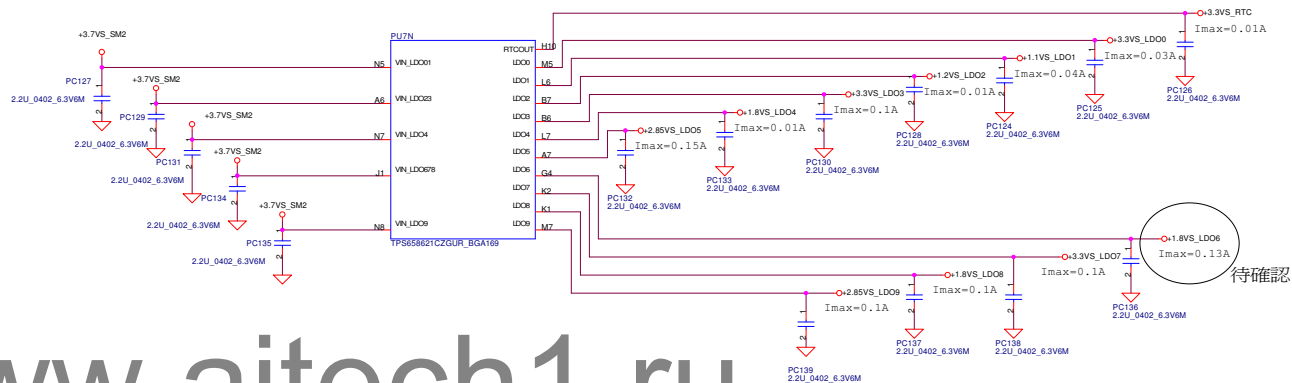
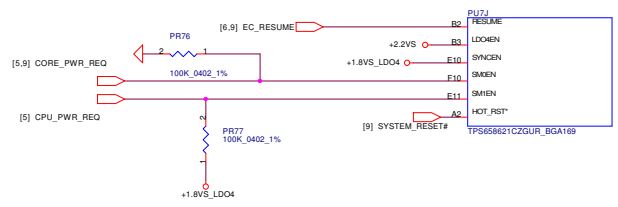
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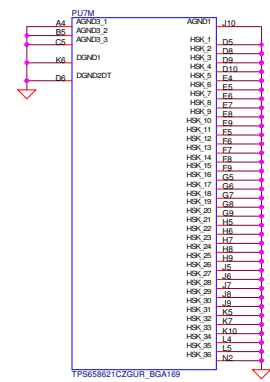
TPS658621\_XTAL1      M5      M6      TPS658621\_XTAL2 [22]



接 整 C  
(POWER BUTTON)



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